IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventer	:	**Pinto et al.**
Application No.	:	**10/561,454**
Filed	:	**December 20, 2005**
For	:	**DATA PROCESSING DEVICE WITH INSTRUCTION CONTROLLED CLOCK SPEED**

APPEAL BRIEF

On Appeal from Group Art Unit 2183

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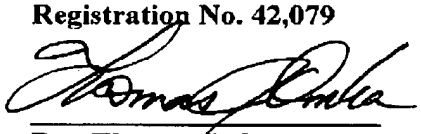

Date: December 16, 2009

By: Thomas J. Onka
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Sir:

In response to a Notification of Non-Compliant Appeal Brief dated November 16, 2009, Appellant submits the following revised "Summary of Claimed Subject Matter" in accordance with M.P.E.P §41.37(d)(B):

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention, particularly, independent claim 1 discloses an instruction controlled data processing device comprising an instruction issue unit (Fig. 1, item 10) that is configured to issue respective ones of instructions of program code in successive instruction cycles (page 4, lines 10-14), the instructions including at least a first type of instruction and a second type of instruction, a clocking circuit (Fig. 1, item 16) that is configured to clock the instruction cycles, a register file (Fig. 1, item 14) with a read port and a write port, a plurality of functional units, (Fig. 1, item 12; Fig. 2, items 20a,b), each functional unit having a control input coupled to the issue unit, an operand input coupled to the read port and a result output coupled to the write port, and a control unit (Fig. 2, item 28) coupled to the issue unit, that is configured to route the result output of a first functional unit (Fig. 2, item 20a) to the write port of the register file in response to instructions of the first type, and to the operand input of a second functional unit (Fig. 2, item 20b) during an instruction cycle in response to instructions of the second type, wherein the clock circuit (Fig. 1, item 16) is configured to vary a rate of clocking the instruction cycles in dependence upon whether a current segment of the program code includes one or more instructions of the second type. (See page 2, lines 9-29; page 3, line 29 – page 4, line 4).

Independent claim 10 discloses a method of executing a processing task, comprising the steps of providing a plurality of functional units, (Fig. 1, item 12; Fig. 2, items 20a,b), issuing successive instructions at an instruction cycle rate, executing those of the instructions that are of a first type each with an individual one of the functional units during one instruction cycle, executing an instruction that is of a second type with a first and a second one of the functional units in series (Fig. 2, items 20a,b) during one instruction cycle, routing a result of the first one of the functional units (Fig. 2, item 20a) to an operand of the second one of the functional units (Fig. 2, item 20b) in response to the instruction of the second type; and selecting the instruction cycle rate from at least a first and second rate, based on the type of instruction, the first rate being so slow that execution of instructions of the second type by a cascade of at least two of the functional units fits within an instruction cycle at the first rate, the second rate being so fast that only execution of instructions of the first type fits within the instruction cycle at the second rate, execution of instructions of the second type not fitting within one instruction cycle at the second rate. (See page 1, line 19 – page 2, line 29; FIG 1; page 3, line 29 – page 4, line 4).

Claims 2 and 4-8 depend from independent claim 1 and recite further aspects of the invention claimed.

Claims 11-12 depend from independent claim 10 and recite further aspects of the invention claimed.

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(Signature and Date) 12/16/09